18 (original). A semiconductor device adapted for stabilizing data storage for a data-storage memory circuit, the semiconductor device comprising:

a thyristor device having a capacitively-coupled control port and anode and cathode end portions, each end portion including an emitter and a base region, the capacitively-coupled control port controlled to switch the thyristor device between a current passing mode and a current blocking mode; and

means for shunting low-level current at a first base region of a first one of the end portions.

19 (original). A semiconductor device adapted for stabilizing data storage for a data-storage memory circuit, the semiconductor device comprising:

a thyristor device having a capacitively-coupled control port and anode and cathode end portions, each end portion including an emitter and a base region, the capacitively-coupled control port controlled to switch the thyristor device between a current passing mode and a current blocking mode; and

a low-level current shunt adapted to shunt current at a first base region of a first one of the end portions.

20 (original). The semiconductor device of claim 19, wherein the low-level current shunt includes a transistor having source and drain regions, one of the source and drain regions being electrically coupled to the emitter region of an end portion of the thyristor device and the other of the source and drain regions being electrically coupled to the base region of the same end portion of the thyristor device, the transistor further having a gate adapted to control the current flow between the source and drain regions.

21 (original). The semiconductor device of claim 20, wherein the gate is electrically coupled to a base region of another end portion of the thyristor device.